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Monolithic Integration of GaN-Based NMOS Digital Logic Gate Circuits with E-Mode Power GaN MOSHEMTs

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***Abstract*— In this work, we demonstrate high-performance NMOS GaN-based logic gates including NOT, NAND, and NOR by integration of E/D-mode GaN MOSHEMTs on silicon substrates. The load-to-driver resistance ratio was optimized in these logic gates by using a multi-finger gate design of E-mode GaN MOSHEMT to increase the logic swing voltage and noise margins, and reduce the transition periods. State-of-the-art NMOS inverter was achieved with logic swing voltage of 4.93 V at a supply voltage of 5 V, low-input noise margin of 2.13 V and high-input noise margin of 2.2 V at room temperature. Excellent high temperature performance, at 300°C, was observed with a logic swing of 4.85 V, low-input noise margin of 1.85 V and high-output noise margin of 2.2V. In addition, GaN-based NAND and NOR NMOS logic gates are reported for the first time with very good performance. Finally, the logic gates were monolithically integrated with high-voltage E-mode power transistors, which reveals a significant step forward towards monolithic integration of GaN power transistors with gate drivers.**

Keywords*— *Logic gates, GaN, high temperature, inverters, NAND, NOR, E-mode, D-mode, monolithic integration

I. INTRODUCTION

The high switching frequency of GaN-based power converters can lead to a significant reduction of the size of passive components, such as capacitors and inductors, and thus, increasing the power density of the overall system [1], [2]. GaN is one of the most promising materials for high frequency power switching due to its exceptional properties such as large saturation velocity, high carrier mobility, and high breakdown field strength. Despite the advantages of GaN power devices, discrete Si-based logic control and gate drivers are still used to control the GaN power devices [3], which limits the switching frequency due to parasitic inductances from external connections of GaN power devices and gate drivers.

A monolithic integration of GaN power devices with GaN-based gate drivers would minimize parasitic components and unveil the full potential of GaN transistors for high frequency power conversion with high efficiency. GaN-based logic gates are essential components to realize level shift, driver control, dead time control and under voltage-lockout (UVLO) for driver circuits. However, high performance CMOS logics in GaN are not feasible today due to the poor transport properties of p-type

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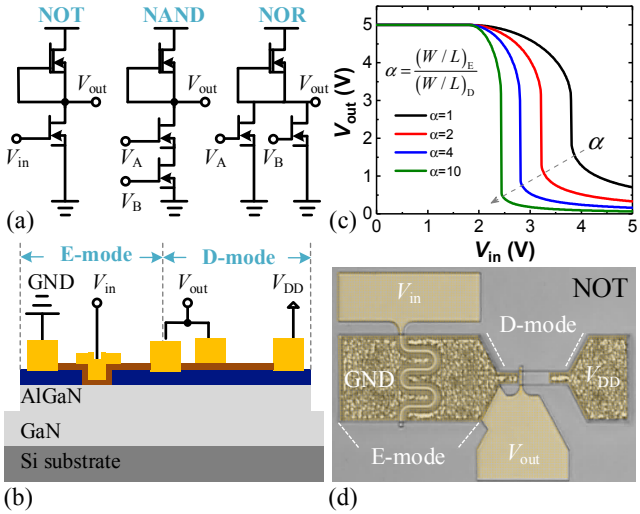

Fig. 1. (a) Equivalent circuits of inverter, NAND and NOR logic gates. (b) Cross-sectional schematic and (c) top view of monolithic integration of E/D-mode MOSHEMTs. (d) Simulated transfer characteristics versus different α ratios.

GaN devices [4], [5]. Ideas to demonstrate purely n-type logic circuits date back of more than 30 years with NMOS logics [6]–[8], also named direct-coupled FET logic (DCFL). GaN DCFLs have been demonstrated [9]–[12], however their performances are not sufficient to satisfy the logic requirements, due to their small noise margins, large logic transition voltages, small logic swing and large low-level output voltages (V_{OL}). Recent research show steady improvements on GaN DCFL [10], however the V_{OL} is still quite high, up to 0.3 V and the maximum voltage swing is 4.66 V, which would lead to high logic losses and safety problems. A very distinct property of GaN compared to Silicon is its high temperature operation, which led to the demonstration of GaN DCFLs operating at high temperatures, up to 375 °C [9], [11], however, it resulted in a much degraded operation compared to room temperature (RT).

In this paper, we demonstrate high-performance NOT, NAND and NOR logic gate units by integrating E/D-mode MOSHEMTs. These logic units were optimized for larger voltage swing, wider noise margin, and smaller transition

periods. High performance was observed even up to 300°C, which could be applied for high temperature applications.

II. Integrated Logic Design and Fabrication

The NMOS logic gate circuits, shown in Fig. 1(a), were fabricated on AlGaN/GaN epitaxial layer on silicon substrate (Fig. 1(b)) consisting of 3.75 µm buffer, 322 nm of un-doped GaN channel, 23.7 nm of AlGaN barrier and 2.4 nm of GaN cap layer. D-mode and E-mode MOSHEMTs were fabricated at the same time, with the sole difference of one additional gate recess process to achieve E-mode operation. To optimize the design of the logics, we simulated the driver-to-load resistance ratio $\alpha = (W/L)_E / (W/L)_D$, as shown in Fig. 1 (c), where W and L are the width and length of the E- and D-mode transistors respectively. Larger values of α result in sharper transitions, higher logic voltage swings and higher noise margins, since the equivalent resistance of E-mode transistor is much smaller than the overall resistance of the circuit. To achieve large values of α, we designed a multi-finger structure for the E-mode MOSHEMT that results in a much smaller resistance of the E-mode compared to the D-mode device without oversizing too much the E-mode transistor (Fig. 1(d)). The chip fabrication started with the definition of the mesa regions by Cl_2-based inductively coupled plasma (ICP) etching. For the E-mode devices, a 1.5 µm-long gate recess was defined by optical lithography and followed by a Cl_2-based slow-rate dry etching, which leads to a precise control of the etching depth. To improve the surface morphology after gate recess, therefore the electron transport of the e-mode devices, we have combined a slow, low-damage ICP etch with a 5%-TMAH wet treatment performed at 80 ºC for 30 minutes (Fig. 2). This step is very critical to obtain a good threshold voltage (V_{th}) control and reasonable on-resistance (R_{dson}) of E-mode transistor. A metal stack of Ti (200 □)/Al (1200 □)/Ti (400 □)/ Ni (600 □)/ Au (500 □) was deposited in the source and drain contact regions by electron-beam evaporation, followed by rapid thermal annealing at 830°C under N_2 atmosphere. The gate dielectric was 25 nm-thick SiO_2 deposited by atomic layer deposition (ALD) at 300°C, immediately after a surface treatment in 37% HCl for 1 min. Finally, gate and contact pads were formed by depositing Ni/Au for both E-mode and D-mode devices. Fig. 1(d) shows the integration of these devices for the NOT logic gate.

III. Results and Discussion

A. DCFL inverter

Fig. 3(a) shows the measured voltage transfer characteristics (VTC) for DCFL inverters with different α, which is consistent with the simulations shown in Fig. 1(c). The performance of the DCFL inverters was characterized with a V_{DD} of 5 V from RT to 300 °C revealing a proper operation with very little variations for this entire temperature range (Fig. 3(b)). The V_{OL} was nearly unchanged, since the

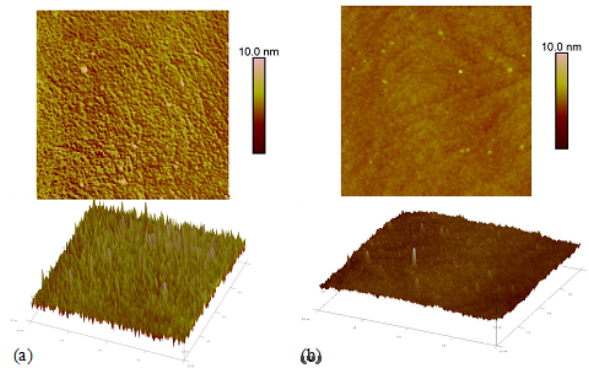

Fig. 2. Surface morphology (a) before and (b) after TMAH treatment.

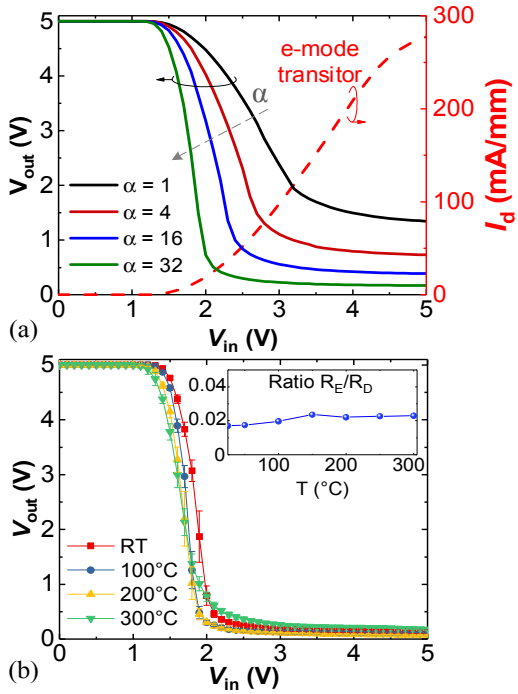

Fig. 3. (a) DCFL VTC versus different α ratio and the transfer characteristics of E-mode transistors (b) DCFL VTC under different temperature varied from RT to 300°C. Inset: resistance ratio of E/D-mode logic versus temperature for output logic equal to 0.

resistance of the E- and D-mode transistors increases at the same rate with temperature (inset of Fig. 3(b)), which results in a nearly constant E/D-mode resistance ratio and thus in a similar V_{OL} since:

$$V_{OL} = \frac{R_E}{R_E + R_D} V_{DD} \quad (1)$$

As shown in Fig. 3(a), the transition voltage of the DCFL inverter is affected by two main factors: the V_{th} of the E-mode transistor and the ratio α. For high performance logics, the ratio α must be as large as possible and the V_{th} of E-mode transistor must be close to $V_{DD}/2 = 2.5$ V in linear scale, which can be controlled by adjusting the gate recess depth.

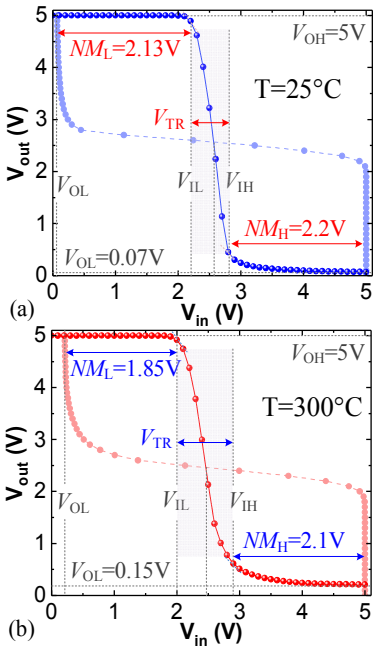

Fig. 4. The VTC of the optimized DCFL inverter with α = 64 at (a) 25°C and (b) 300°C with supply voltage V_{DD}=5V.

We optimized the design of the DCFL inverter by integrating a D-mode MOSHEMT with $(W/L)_E$ = 160 μm/8 μm acting as the active load and an D-mode MOSHEMT with a $(W/L)_E$ = 10 μm/32μm acting as the driver source, which corresponds to a ratio α of 64. By adjusting the gate recess from 25 nm to 27 nm, the V_{th} of the E-mode transistor was increased from 1.8 V (Fig.2 (a)) to 2.5 V in linear scale. The VTCs of the optimized DCFL inverter are shown in Fig. 54. The high-level output voltage (V_{OH}) and V_{OL} were 5 V and 0.07 V, respectively, yielding a much larger voltage swing of 4.93 V/5 V (98.6%) compared to the best values in the literature of 4.66 V/5 V (93.2%) [10] and 6.3 V/7 V (90%) [13]. The low-level input voltage (V_{IL}) and high-level input voltage (V_{IH}), defined at dV_{out}/dV_{in} = -1, were 2.2 V and 2.8 V respectively. The VTC consist of three main regions: the low-input region at $v_{in}<V_{IL}$, the transition region at $V_{IL}\le v_{in}\le V_{IH}$, and the high-input region at $v_{in}>V_{IH}$. The width of the transition voltage region (V_{TR}= V_{IH} - V_{IL}) is a way of measure the ambiguity of the logic inverter [14], which must be as low as possible. The transition voltage width was 0.6 V/5 V (12%) in our case, which is smaller than the lowest values in the literature 1 V/5 V (20%) [10] and 1.6 V/7 V (22%) [13]. The low-input-logic noise margin (NM_L=V_{IL} - V_{OL}) and high-input-logic noise margin (NM_H=V_{IH} - V_{OH}) are 2.13 V/ 2.5V (85.2%) and 2.2 V/2.5 V (88%) respectively, which outperforms the best values of 1.7 V/2.5 V (68%) and 2 V/2.5 V (80%) in [10].

High temperature performance of this inverter is shown in Fig. 54(b), revealing a very good behavior at 300 °C with V_{OH}, V_{OL}, V_{IL}, V_{IH} equal to 5 V, 0.15 V, 2 V, 2.9 V, respectively. The voltage swing at 300 °C was 4.85 V/5 V (97%), with 1.6% degradation compared with the value at RT. This value

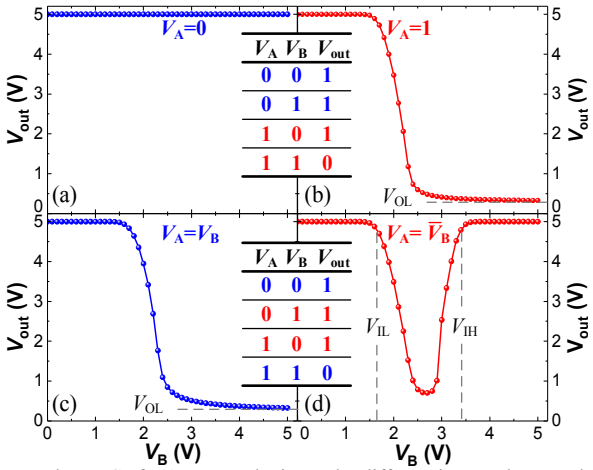

Fig. 5. The VTC of NAND gate logics under different input voltages, where (a) V_A = 0, (b) V_A = 1, (c) V_A =V_B, and (d) V_A= $\overline{V}_B$, V_B is sweeping from 0 to 5V. Insets: corresponding truth table for NAND logic.

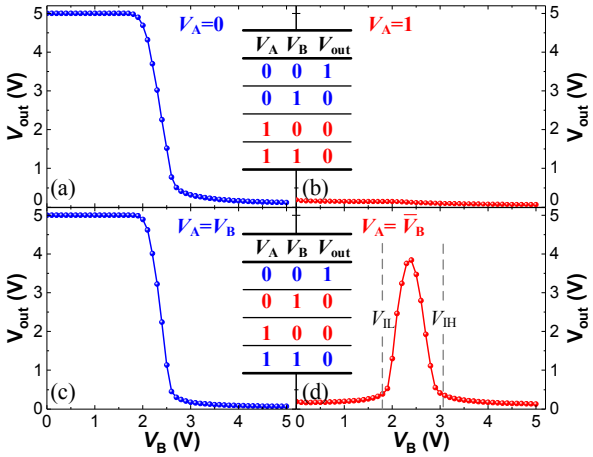

Fig. 6. The VTC of NOR gate logics under different input voltages, where (a) V_A = 0, (b) V_A = 1, (c) V_A =V_B, and (d) V_A= $\overline{V}_B$, V_B is sweeping from 0 to 5V.

is much larger than the best values in the literatures 4.5 V/5 V (90%) in [10] at 200°C and 6.5 V/7 V (93%) in [11] at 300°C. NM_L and NM_H at 300°C were 1.85 V/2.5 V (74%) and 2.1 V/2.5V (84%), respectively, which shows an excellent operation even at 300°C.

B. NAND and NOR logic gate

Fig. 5 shows the VTC of the fabricated NAND logic gates (equivalent circuit in Fig. 1(a)), for which V_{DD} was 5 V, V_B was swept from 0 to 5V and V_A was set at 4 different cases:

case 1: *V_A=0, thus $V_{out} = \overline{V}_A + \overline{V}_B = 1$ (Fig. 5 (a));*

case 2: *V_A=1, thus $V_{out} = \overline{V}_A + \overline{V}_B = \overline{V}_B$ (Fig. 5 (b)). The V_{OL} = $2R_E/(R_D+2R_E)\cdot V_{DD}$ is larger than that of the inverter since the equivalent resistance of E-mode transistor is $2R_E$ instead of R_E.*

case 3: *V_A=V_B, thus $V_{out} = \overline{V}_A + \overline{V}_B = \overline{V}_B + \overline{V}_B$. In this case, V_A and V_B are changing simultaneously, which is quite similar to the case 2 (Fig. 5(c)), except that the transition*

region is relatively longer, since the equivalent resistance in the lower side is larger;

case 4: $V_A = \overline{V}_B$, *thus* $V_{out} = \overline{V}_A + \overline{V}_B = V_B + \overline{V}_B$, *(Fig. 5(d)). When* $V_B < V_{IL}$ *and* $V_B > V_{IH}$, V_B*=0 and* V_B*=1, thus* V_{out}*=1, and* $V_{IL} \le V_B \le V_{IH}$*, the logic output is ambiguous.*

Fig. 6 shows the VTC of the fabricated NOR logic gates (equivalent circuit in Fig. 1(a)), for which V_A was set at 4 different cases:

case 1: V_A*=0, thus* $V_{out} = \overline{V}_A \cdot \overline{V}_B = \overline{V}_B$ *(Fig.5 (a)).*

case 2: V_A*=1, thus* $V_{out} = \overline{V}_A \cdot \overline{V}_B = 0$ *(Fig.5 (b)).*

case 3: $V_A = V_B$, *thus* $V_{out} = \overline{V}_A \cdot \overline{V}_B = \overline{V}_B \cdot \overline{V}_B$. *In this case,* V_A *and* V_B *are changing simultaneously, which is quite similar to case 1 (Fig. 6(c)), except that the equivalent resistance is* $R_E/2$ *instead of* R_E*, which led to a lower* V_{OL} *and sharper transition.*

case 4: $V_A = \overline{V}_B$, thus $V_{out} = \overline{V}_A \cdot \overline{V}_B = V_B \cdot \overline{V}_B$ (Fig. 6(d)). When $V_B < V_{IL}$ and $V_B > V_{IH}$, V_B=0 and V_B=1, thus V_{out}=0. When $V_{IL} \le V_B \le V_{IH}$, the logic output is ambiguous.

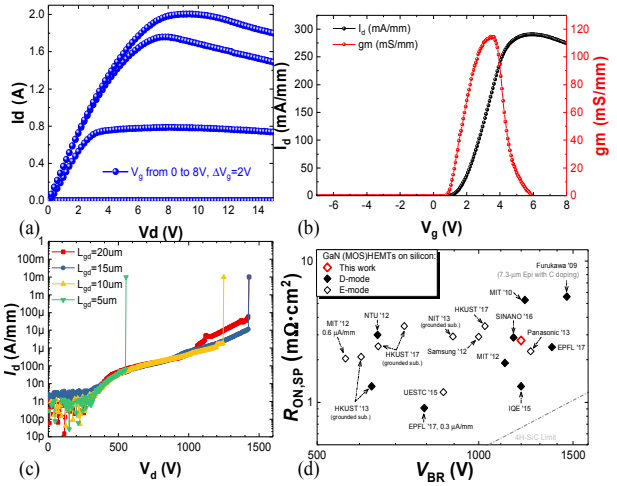

Fig. 7. (a) The output, (b) transfer characteristics, (c) breakdown voltage and (d) benchmark of E-mode power GaN MOSHEMT

C. Logic intergrated with E-Mode power MOSHEMTs

In order to demonstrate the probability of integration with GaN logic with power transistors, we fabricate them on same wafer. The E-mode power MOSHEMTs fabricated on the same chip as the logic gates, presented low leakage current, threshold voltage of 1.5V, and high breakdown voltage (up to 1400V) (Fig. 7). Our integrated E-mode power GaN MOSHEMTs was benchmarked against state-of-the-art GaN MOSHEMTs on Si (Fig. 7(d)).

IV. Conclusion

In this paper, we have demonstrated high performance NOT logic with high logic swing voltage, high noise margin, and low transition period both at RT and at 300°C. NAND and NOR GaN logic gates were demonstrated for the first time with very good performance. E-mode power MOSHEMTs with 1kV breakdown and 2A current capability were fabricated on the same chip as the logic gates. These results show the enormous potential of GaN-based logic gates for future monolithic integration in gate drivers as well as for high temperature applications.

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